

CLAIMS

What is claimed is:

1. A sublamination layer, comprising:
 - 5 a single layer etched reference plane having a top surface and a bottom surface;
 - a first signal layer coupled to the top surface with a first bond-ply material;
 - a second signal layer coupled to the bottom surface with a second bond-ply material;
 - and
 - at least one of a through via.
- 10 2. The sublamination layer of claim 1, wherein the single layer etched reference plane comprises a metal.
3. The sublamination layer of claim 2, wherein the metal is copper or nickel.
4. The sublamination layer of claim 1, wherein the first bond-ply material and the second bond-ply material comprise a same materials.
- 15 5. The sublamination layer of claim 4, wherein the same material is FR4 or cyanate ester.
6. The sublamination layer of claim 1, wherein the first bond-ply material and the second bond-ply material do not comprise a same material.
7. An electronic component comprising the sublamination layer of claim 1.
8. The electronic component of claim 7, wherein the electronic component is a printed circuit board.
- 20 9. An electronic product comprising the sublamination layer of claim 1.
10. A method of producing a sublamination layer, comprising
 - providing an unsupported layer of material having a top side and a bottom side;
 - applying a photoactive resist to the top side and the bottom side of the material;
 - 25 exposing the top side and the bottom side with a light image;
 - removing the photoactive resist material that is not exposed;
 - etching the unsupported layer of material;
 - cleaning the unsupported layer of material;
 - coupling a bonding material to the top side and bottom side of the unsupported layer;
 - 30 coupling a first signal layer to the bonding material coupled to the top side; and
 - coupling a second signal layer to the bonding material coupled to the bottom side.

11. The method of claim 10, wherein the unsupported layer of material comprises a metal.
12. The method of claim 11, wherein the metal is copper or nickel.
13. The method of claim 11, wherein the bonding material is FR4 or triazine/bismaleimide.
- 5 14. A method for producing an electronic component, comprising:
providing a substrate;
coupling at least one sublamination material to the substrate; and
coupling at least one additional layer to the sublamination material.
15. The method of claim 14, wherein the substrate is a silicon wafer.
- 10 16. The method of claim 14, wherein the sublamination material is the sublamination material of claim 1.
17. The method of claim 14, wherein the additional layer is a laminate.
18. The method of claim 14, wherein the electronic component comprises a printed circuit board.

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